What is claimed is:

1. A semiconductor device, comprising:

a plurality of metal line patterns having a predetermined surface area size, wherein two adjacent metal line patterns are spaced apart from each other at a predetermined distance.

2. A semiconductor device as claimed in claim 1, wherein the predetermined distance is greater than 1.0 μm.

3. A semiconductor device as claimed in claim 1, wherein the predetermined distance is greater than 1.5 μm.

4. A semiconductor device as claimed in claim 1, wherein the plurality of metal line patterns have a surface area size of greater than "30μm×30μm".

5. A semiconductor device, comprising:

a metal line layer having a plurality of metal line patterns spaced apart from each other; and

at least one underlying layer under the metal line layer,

wherein the space between two adjacent metal line patterns has a sufficient width to prevent a crack from occurring in the underlying layer.

6. A semiconductor device as claimed in claim 5, wherein the width of the space is greater than 1.0 μm.

7. A semiconductor device as claimed in claim 5, wherein the width of the space is greater than 1.5 μm.

8. A semiconductor device as claimed in claim 5, wherein the underlying layer is an insulating layer.

9. A semiconductor device as claimed in claim 5, wherein the metal line pattern has a surface area size of greater than "30μm×30μm".

10. A semiconductor device, comprising:

a plurality of metal line patterns, wherein two adjacent metal line patterns are spaced apart from each other, and at least one of the two adajacent metal line patterns has a slit.

11. A semiconductor device as claimed in claim 10, wherein the slit has a width of greater than 1.0 μm.

12. A semiconductor device as claimed in claim 11, wherein the slit is formed at a predetermined distance from an edge of the metal line pattern.

13. A semiconductor device as claimed in claim 12, wherein the predetermined distance is less than 4 μm.

14. A semiconductor device having a multi-layered structure, comprising:

a metal line layer having a plurality of metal line patterns spaced apart from each other;

at least one underlying layer under the metal line layer; and

a slit formed at a sufficient distance from a space between two adjacent metal line patterns to prevent a crack from occurring in the underlying layer.

15. A semiconductor device as claimed in claim 14, wherein the slit is formed in a direction parallel to the space between two adjacent metal line patterns.

16. A semiconductor device as claimed in claim 14, wherein the slit has a width greater than 1.0 μm.

17. A semiconductor device as claimed in claim 14, wherein the distance from the space between the two adjacent metal line patterns to the slit is less than 4.0 μm.

18. A method of manufacturing a semiconductor device having a multi-layered structure, comprising:

forming at least one underlying layer on a semiconductor substrate; and

forming a metal line layer on the underlying layer, the metal line layer having a plurality of metal line patterns spaced apart from each other at a predetermined distance.

19. A method as claimed in claim 18, wherein the predetermined distance is greater than 1.0 μm.

20. A method as claimed in claim 18, wherein the predetermined distance is greater than 1.5 μm.

21. A method of manufacturing a semiconductor device having a multi-layered structure, comprising:

forming at least one underlying layer on a substrate;

forming simultaneously a metal line layer on the underlying layer and a slit, the metal line layer having a plurality of metal line patterns spaced apart from each other, at least one of either of two adjacent metal lines has a slit.

22. A method as claimed in claim 21, wherein the slit is formed in a direction parallel to the space between two adjacent metal line patterns.

23. A method as claimed in claim 21, wherein a width of the slit is greater than 1.0 μm.

24. A method as claimed in claim 21, wherein a distance from the space between two adjacent metal line patterns to the slit is less than 4.0 μm.

25. A method of manufacturing a semiconductor device, comprising:

forming at least one underlying layer on a substrate;

forming simultaneously a metal line layer on the underlying layer and a slit, the metal line layer having a plurality of metal line patterns spaced apart from each other, the slit formed at a sufficient distance from a space between the two adjacent metal line patterns in order to prevent a crack from occurring in the underlying layer.

26. A method as claimed in claim 25, wherein the slit is formed in a direction parallel to the space between two adjacent metal line patterns.

27. A method as claimed in claim 25, wherein the width of the slit is greater than 1.0 μm.

28. A method as claimed in claim 25, wherein the distance between the slit and the space between two adjacent metal line patterns is less than 4.0 μm.